REMARKS

In response to the official action:

§ 112. The claims were rejected under the second paragraph for reciting *a target element whose dielectric loss is to be controlled among the at least one element*. This rejection is respectfully traversed.

Dielectric Loss. As the Examiner is aware, virtually all non-metallic materials are dielectrics; whenever there is a varying electromagnetic field in the dielectric there is a loss; and this loss can be controlled by various methods (for example, by changing the frequency of the electromagnetic field or by changing the amount of dielectric). Thus, almost every electronic device will have a dielectric loss that can be controlled. In the Background section, the Applicants discuss parasitic capacitance, which is especially important at high frequencies because even a small capacitance will pass high frequencies easily, so that stray capacitance will cause leakage at high frequency.

The Examiner will recall that in the case of a parallel-plate capacitor, a dielectric increases the capacitance. In the case of other devices, the presence of dielectric also increases the capacitance (in this case, parasitic capacitance). For example, an isolated electrical terminal will have a certain capacitance relative to ground potential, but, if the space surrounding the terminal is filled with a dielectric such as oil, the capacitance will be increased; similarly, if a piece of solid dielectric is placed near to the terminal, the capacitance of the terminal will be increased. When the capacitance is increased, a high-frequency voltage present on the terminal will more easily leak to ground and cause more loss.

The Examiner will appreciate that in the Applicants' Fig. 2, the groove G under transistor 6a (the target element) represents an absence of dielectric (dielectric that would have been there without the Applicants' invention), which decreases the parasitic capacitance and therefore the

loss. This is believed to answers the Examiner's question about how the target element has a dielectric loss.

Target Element. The Examiner is invited to consider that when someone makes a semiconductor device, she or he may (or may not) know in advance that a target element is formed on the SOI layer. If she identifies a target element on the SOI layer (this is mentioned in instant claim 9), then she can make the claimed groove in the substrate under the target element. In the Detailed Description, the target element is exemplified as an inductor, a high-frequency circuit, and an analog circuit—any element can be a target element as long as that element will cause a dielectric loss, and how the target is selected may be a matter of judgment or engineering.

The Examiner is invited to note that claim 1 is an apparatus claim that defines the *structure* of the semiconductor device, rather than being a method claim for *making* a semiconductor device. Therefore, claim 1 is not required to set forth how to determine the target element, or whether it has a dielectric loss (although, as noted above, almost every element has some dielectric loss). Because parasitic capacitance loss is a function of frequency as well as structure, the same structure could be a target or not, depending on the frequency of the signal. If claim 1 were a method claim instead of an apparatus claim, then it might include a step for determining whether the target element exists on the SOI layer—but it is not, and therefore need not include such a step.

For the record, the Applicants argue that claim 1 does not have to recite *why* the groove can reduce the dielectric loss or *how* to reduce the dielectric loss of the target element, because claim 1 is absolutely definite as long as the claimed structure is clear.

Claim 6. In claim 1, the phrase "at least one element" covers just one element formed on the SOI layer, or a plurality of such elements. The Applicants' claim 1 implies that a semiconductor device manufacturing person can select a target element formed on the SOI layer. But, as mentioned above, this is not a structural feature and "target" merely defines to a subset

(which can be a proper or an improper subset) of the elements. Such a subset is a structural feature, and subsets are commonly referred to in apparatus claims by using terminology such as "predetermined." In claim 6, a subset is referred to as "one or more analog elements among the plurality of elements."

Under claim 6, if the manufacturing person knows a certain analog element will cause a dielectric loss, then he or she can designate such an analog element as a target element and then make a groove in the substrate beneath it. But, with respect, no method of selecting "one or more analog elements among the plurality of elements" is required in the claim.

§ 102. Claims 1-3, 5-7, and 10 were rejected as being as anticipated by Yonehara '266. This rejection is respectfully traversed.

The independent claims are amended to recite additional layers (exemplified by layers 5-2 and 5-3 in instant Fig. 2) and an additional insulation layer (exemplified by layers 5b in instant Fig. 2), and also recite that the device is non-optical. These features distinguish over Yonehara.

The Examiner is invited to further consider that Yonehara discloses grooves, but these grooves are used to provide light transmission and are placed under optical elements (liquid crystal pixels). Therefore, the location of the Yonehara groove will be different from the location of the groove claimed by the Applicants—the target will be different, and therefore the structure will be different.

With respect, the rejection errs in stating that Yonehara discloses "a target element (57) whose dielectric loss is to be controlled." The paragraph explaining Fig. 38, in which element 57 appears (col. 50, lines 26-44) does not mention dielectric loss, much less controlling any dielectric loss.

§ 103. Claims 4 and 8 were rejected as obvious under Yonehara in view of Edo '057. This rejection is respectfully traversed.

The Examiner admits that Eda does not show a groove below the inductor 5 (col. 11, line 27). Instead, there is a hollow below the quartz crystal 2, which is there to provide an electrode 7 on the lower surface of the crystal. No mention of dielectric loss is seen.

Even if one were to add an inductor to Yonehara (not admitted obvious), Yonehara would not put the inductor in the light path, because that would obstruct the light. It would be put somewhere else. And if put somewhere else, there would be no groove under it because neither reference teaches putting a groove under an inductor, which is neither an optical window nor a quartz crystal.

There is no motivation to combine the references. With respect, providing an inductor "to act as a passive chip component," as the Examiner asserts, is not sufficient as Yonehara expresses no need for passive chip components and the person of ordinary skill would not add one of these to Yonehara arbitrarily, for no reason.

The new feature recited in the claims, namely the additional layers, is contrary to the optical function of Yonehara because the additional layers would block light.

Respectfully submitted,

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I certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office (fax no. 571-273-8300) on August 3, 2005.

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